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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2181	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/750,150	HAMMOND ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12 and 14-22 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 07/02/2007.

Claim Rejections - 35 USC § 101

3. The examiner acknowledges the applicant's amendment to the specification to remove the "radio frequency link" example of machine readable medium from the specification. However, the inclusion of the "radio frequency link" example (as well as any medium that can transfer data; See paragraph 36 of specification) in the specification as originally filed indicates that the applicant intends for a machine readable medium to include a signal. Therefore, removal of the "radio frequency link" example alone does not overcome the rejection under 35 U.S.C. 101. If the applicant does not intend to for the claimed machine readable medium to include a signal, then the applicant must make a clear disavowal of intent to claim a signal.

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 17-21 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 17-21 recite a "machine readable medium", which is defined within the specification (paragraph 36 on page 12) as "any medium that can store or transfer information. Examples of a machine readable medium include... a radio frequency (RF) link, and similar media and mediums."

Therefore, it is understood that applicant intends for a machine readable medium to include a signal (e.g. radio frequency link). An analysis of a signal per se done in accordance with the "Interim Guidelines for Examination of Patent Applications for Patent Subject Matter Eligibility" concludes that a signal per se is not a process, machine, composition of matter, nor manufacture and, therefore, does not fall within any of the categories of patentable subject matter set forth in 35 U.S.C. 101. Therefore, claims 17-21 claim non-statutory subject matter.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-10 and 14-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Gharachorloo et al., "Two Techniques to Enhance the Performance of Memory Consistency Models" (Hereinafter Gharachorloo).

8. Referring to claim 1, Gharachorloo has taught a method comprising:

issuing a load instruction to an execution cluster *[function units; Fig. 3]* in an out of order processor *[2nd paragraph of section 4.2 on page 5]*;

allocating an entry for the load instruction in a structure *[speculative-load buffer; Fig. 4]* for tracking only load instructions, if the load instruction utilizes speculative data *[3rd full paragraph, right column, page 6]*; and

flagging a field in a reorder buffer *[Fig. 3]* to indicate the load instruction that uses speculative data is to be checked at retirement, the field in an entry tracking program order of the load instruction *[Each instruction, including the load instruction, is allocated a location in the reorder buffer (2nd full paragraph, right column, page 5). That is, an entry (location) in the reorder buffer is flagged. This location tracks the program order of the instruction (3rd full paragraph, right column, page 5)]*.

9. Referring to claim 2, Gharachorloo has taught the method of claim 1, further comprising:

searching the structure to confirm the load data at the time of retirement *[3rd full paragraph, right column, page 6]*.

10. Referring to claim 3, Gharachorloo has taught the method of claim 1, further comprising:

invalidating the entry for the load instruction during a store instruction retirement if the store instruction conflicts with the load instruction *[last paragraph, right column, page 6]*.

11. Referring to claim 4, Gharachorloo has taught the method of claim 2, further comprising:

flushing the pipeline if the structure for tracking only load instructions does not contain a valid entry for the load instruction at load instruction retirement *[3rd full paragraph, left column, page 7]*.

12. Referring to claim 5, Gharachorloo has taught the method of claim 1, wherein the load instruction is an advanced load instruction *[The load instruction has been*

advanced in front of a store instruction; 2nd and 3rd full paragraphs, right column, page 6].

13. Referring to claim 6, Gharachorloo has taught the method of claim 5, further comprising:

converting a basic load instruction into an advanced load instruction *[By advancing the load instruction in front of a store instruction the load instruction is converted into an advanced load instruction; 2nd and 3rd full paragraphs, right column, page 6].*

14. Referring to claim 7, Gharachorloo has taught the method of claim 1, wherein the structure for tracking load instructions is an advanced load allocation table *[The speculative-load buffer is a table that allocates entries for speculative advanced load instructions (2nd and 3rd full paragraphs, right column, page 6) and is, therefore, an advanced load allocation table].*

15. Referring to claim 8, Gharachorloo has taught a device comprising:

a store queue *[store buffer; Fig. 4]* in an out of order processor to track only store instructions *[3rd paragraph, left column, page 6]*;

a load queue *[speculative-load buffer; Fig. 4]* coupled to the store queue to track only speculative load instructions *[3rd full paragraph, right column, page 6]*; and

a reorder buffer *[Fig. 3]* to track program order of instructions *[2nd full paragraph, right column, page 5]*, the reorder buffer including an entry to track program order of a load instruction *[Each instruction, including the load instruction, is allocated a location in the reorder buffer (2nd full paragraph, right column, page 5) that tracks the program*

order of the instruction (3rd full paragraph, right column, page 5)], the entry including a field indicating the load instruction is to be checked at retirement *[The location allocated to an instruction in the reorder buffer is a field that indicates that the instruction is to be checked at retirement (3rd full paragraph, right column, page 5)]*.

16. Referring to claim 9, Gharachorloo has taught the device of claim 8, further comprising:

an instruction scheduler *[load/store reservation station; Fig. 4]* coupled to the store queue to schedule instruction execution *[3rd paragraph, left column, page 6]*.

17. Referring to claim 10, Gharachorloo has taught the device of claim 8, wherein the load queue is an advanced load allocation table *[The speculative-load buffer is a table that allocates entries for speculative advanced load instructions (2nd and 3rd full paragraphs, right column, page 6) and is, therefore, an advanced load allocation table]*.

18. Referring to claim 14, Gharachorloo has taught an apparatus comprising:

means for tracking only speculative load instructions *[speculative-load buffer; Fig. 4; 3rd full paragraph, right column, page 6]*; and

means for tracking all instructions in program order *[reorder buffer; Fig. 3; 2nd full paragraph, right column, page 5]* coupled to the means for tracking only speculative load instructions, comprising a field to indicate a load instruction is to be checked at retirement, the field in an entry tracking program order of the load instruction *[Each instruction, including the load instruction, is allocated a location in the reorder buffer (2nd full paragraph, right column, page 5) that tracks the program order of the instruction (3rd full paragraph, right column, page 5). The location allocated to an instruction in the*

reorder buffer is a field that indicates that the instruction is to be checked at retirement (3rd full paragraph, right column, page 5)].

19. Referring to claim 15, Gharachorloo has taught the apparatus of claim 14, further comprising:

means for tracking only store instruction coupled to means for tracking only speculative load instructions *[store buffer; Fig. 4; 3rd paragraph, left column, page 6].*

20. Referring to claim 16, Gharachorloo has taught the apparatus of claim 14, further comprising:

means for flushing a pipeline upon detection that a speculative load is not present in the means for tracking only speculative loads at the time of load instruction retirement *[3rd full paragraph, left column, page 7].*

21. Referring to claim 17, Gharachorloo has taught a machine readable medium having instructions stored therein which when executed cause a machine to perform a set of operations comprising:

tracking only a set of load instructions relying on speculative data in a first data structure *[speculative-load buffer; Fig. 4; 3rd full paragraph, right column, page 6]* of an out of order processor *[2nd paragraph of section 4.2 on page 5]*; and

tracking a set of instructions in program order in a second data structure *[reorder buffer; Fig. 3; 2nd full paragraph, right column, page 5]* having a field to indicate to check speculation in a load instruction at a time of load instruction retirement, the field in an entry tracking program order of the load instruction *[Each instruction, including a speculative load instruction, is allocated a location in the reorder buffer (2nd full*

paragraph, right column, page 5) that tracks the program order of the instruction (3rd full paragraph, right column, page 5). The location allocated to an instruction in the reorder buffer is a field that indicates that the instruction is to be checked at retirement (3rd full paragraph, right column, page 5)].

22. Referring to claim 18, Gharachorloo has taught the machine readable medium of claim 17, having instructions stored therein which when executed causes a machine to perform a set of operations further comprising:

tracking only a set of store instructions in a store queue *[store buffer; Fig. 4]* of the out of order processor *[3rd paragraph, left column, page 6].*

23. Referring to claim 19, Gharachorloo has taught the machine readable medium of claim 17, having instructions stored therein which when executed cause a machine to perform a set of operations further comprising:

invalidating allocated load instruction entries during store instruction retirement *[last paragraph, right column, page 6].*

24. Referring to claim 20, Gharachorloo has taught the machine readable medium of claim 17, wherein the first data structure is an advanced load allocation table *[The speculative-load buffer is a table that allocates entries for speculative advanced load instructions (2nd and 3rd full paragraphs, right column, page 6) and is, therefore, an advanced load allocation table].*

25. Referring to claim 21, Gharachorloo has taught the machine readable medium of claim 17, wherein the second data structure is a reorder buffer *[Fig. 3; 2nd full paragraph, right column, page 5].*

Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gharachorloo in view of Huck et al., "Introducing the IA-64 Architecture" (Hereinafter Huck).

28. Referring to claim 11, Gharachorloo has taught a system comprising:

a first processor comprising

a first data cache *[D-Cache; Fig. 3]*,

a set of execution units *[function units; Fig. 3; 2nd paragraph on section 4.2 on page 5]*,

an out-of-order instruction scheduler *[reservation stations; Fig. 3]* coupled to the data cache and the set of execution units *[2nd paragraph of section 4.2 on page 5]*,

a store queue *[store buffer; Fig. 4]* coupled to the instruction scheduler to track only store instructions *[3rd paragraph, left column, page 6]*,

a load queue *[speculative-load buffer; Fig. 4]* coupled to the store queue to track only speculative load instructions *[3rd full paragraph, right column, page 6]*,

a reorder buffer *[Fig. 3]* to track program order of instructions *[2nd full paragraph, right column, page 5]*, the reorder buffer including an entry to track the program order of a load instruction *[Each instruction, including the load instruction, is allocated a location in the reorder buffer (2nd full paragraph, right column, page 5) that tracks the program order of the instruction (3rd full paragraph, right column, page 5)]*, the entry including a field indicating the load instruction is to be checked at retirement *[The location allocated to an instruction in the reorder buffer is a field that indicates that the instruction is to be checked at retirement (3rd full paragraph, right column, page 5)]*;

a bus coupled to the processor *[bus between data memory and D-Cache; Fig. 3]*; and

a system memory device *[data memory; Fig. 3]* coupled to the bus.

Gharachorloo has not explicitly taught that the processor has at least a 64 bit architecture.

Huck has taught a processor having a 64-bit architecture *["Architectural basics" section on pages 12 and 13]*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have modified the processor of Gharachorloo to have a 64-bit architecture.

The suggestion/motivation for doing so would have been that the address space is advantageously increased *[1st paragraph of "IA-64 virtual memory model" section on page 17].*

29. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gharachorloo in view of Huck et al., "Introducing the IA-64 Architecture" (Hereinafter Huck), and, further, in view of examiner's taking of Official Notice.

30. Referring to claim 12, Gharachorloo and have taught the system of claim 11 further comprising:

a second processor coupled to the bus comprising a second data cache *[The first processor is part of a multiprocessor (3rd paragraph, left column, page 6). Therefore, there is inherently a second processor that is coupled to the bus].*

Gharachorloo is silent on the implementation of the other processors in the multiprocessor and, therefore, has not explicitly taught that the second processor comprises a second data cache.

However, Examiner takes Official Notice that including a data cache in a processor is conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second processor of Gharachorloo to comprise a data cache since doing so would reduce the latency of data accesses.

31. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gharachorloo in view of Yoaz et al., "Speculation Techniques for Improving Load Related Instruction Scheduling" (Hereinafter Yoaz).

32. Referring to claim 22, Gharachorloo has taught a method comprising:

allocating a first entry for a load instruction in a reorder buffer *[Fig. 3; 2nd paragraph, right column, page 5]*, the first entry to track program order of the load instruction *[3rd paragraph, right column, page 5]*;

issuing the load instruction to an execution cluster *[function units; Fig. 3]* in an out of order processor *[2nd paragraph of section 4.2 on page 5]*;

allocating a second entry for the load instruction in a load table *[speculative-load buffer; Fig. 4]*, the load table being a structure for tracking only load instructions, the second entry including characteristics of an operation of the load instruction *[3rd paragraph, right column, page 6]*; and

flagging a field in the first entry in the reorder buffer, the field to indicate that the load instruction is to be checked at retirement of the load instruction *[Each instruction, including the load instruction, is allocated a location in the reorder buffer (2nd paragraph, right column, page 5). That is, an entry (location) in the reorder buffer is flagged]*.

Gharachorloo has not explicitly taught: determining that it is unknown whether a memory address associated with a store instruction that is prior, in program order, to the load instruction conflicts with a memory address associated with the load instruction; utilizing speculative data in an execution of the load instruction by the out of order processor, if it is determined that it is unknown whether the memory address associated

with the store instruction conflicts with the memory address associated with the load instruction; checking the load instruction in relation to the load table at retirement, to confirm accuracy of the speculative data used in the execution of the load instruction.

Yoaz has taught: determining that it is unknown whether a memory address associated with a store instruction that is prior, in program order, to the load instruction conflicts with a memory address associated with the load instruction *[Yoaz; 2nd paragraph of section 1; 1st paragraph of section 2.1]*; utilizing speculative data in an execution of the load instruction by the out of order processor, if it is determined that it is unknown whether the memory address associated with the store instruction conflicts with the memory address associated with the load instruction *[Yoaz; 1st paragraph of section 2.1]*; checking the load instruction in relation to the load table at retirement, to confirm accuracy of the speculative data used in the execution of the load instruction *[Yoaz; top of page 46, right column (i.e. point # 4)]*.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify the method of Gharachorloo to further include determining that it is unknown whether a memory address associated with a store instruction that is prior, in program order, to the load instruction conflicts with a memory address associated with the load instruction; utilizing speculative data in an execution of the load instruction by the out of order processor, if it is determined that it is unknown whether the memory address associated with the store instruction conflicts with the memory address associated with the load instruction; checking the load instruction in

relation to the load table at retirement, to confirm accuracy of the speculative data used in the execution of the load instruction as taught by Yoaz;

The motivation for doing so would have been that higher performance is achieved *[Yoaz; last paragraph of section 1.1 on page 43, right column].*

Response to Arguments

33. Applicant's arguments filed 07/02/2007 have been fully considered but they are not persuasive.

34. Applicant argues the novelty/rejection of claims 1-12 and 14-21 in substance that Gharachorloo does not teach "flagging a field in a reorder buffer to indicate the load instruction that uses speculative data is to be checked at retirement, the field in an entry tracking program order of the load instruction" (page 8 of arguments). In particular, the applicant asserts that the location in the reorder buffer that is allocated for the load instruction is not flagged to indicate that the instruction is to be checked at retirement. The examiner disagrees with this assertion. It appears to the examiner that the applicant is reading the cited claim limitation too narrowly. Gharachorloo has taught allocating a location (i.e. the writing, or flagging, of a field) in the reorder buffer for each instruction (2nd paragraph, right column, page 5) wherein the location tracks the program order of the instruction (3rd paragraph, right column, page 5). By allocating a location in the reorder buffer, it is indicated that the instruction is to be checked at retirement (1st paragraph, right column, page 6). Therefore, Gharachorloo has taught "flagging a field in a reorder buffer to indicate the load instruction that uses speculative

data is to be checked at retirement, the field in an entry tracking program order of the load instruction".

35. Applicant's arguments with respect to claim 22 have been considered but are moot in view of the newly found reference Yoaz.

Conclusion

36. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Benjamin P Geib
Examiner
Art Unit 2181

ALFORD KINDRED
PRIMARY EXAMINER